	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	68	gate and interlayer and barrier and seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 22:12			0
2	BRS	L2	1	gate and interlayer and via with barrier with seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 22:14			0
3	BRS	L3	2	dram and interlayer and via with barrier with seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 22:18			0
4	BRS	L4	0	source and drain and memory and interlayer and via with barrier and seed with electrode and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 22:20			0
5	BRS	L5	13	source and drain and memory and plug with barrier and seed with electrode and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 22:39			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
6	BRS	L6	0	source and drain and memory and plug with barrier and seed adj electrode and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 22:40			0
7	BRS	L7	6	source and drain and memory and plug with barrier and seed adj3 electrode and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 22:40			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	0	mos with interlayer and barrier with seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 00:36			0
2	BRS	0	mos with interlayer and barrier and seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 00:37			0
3	BRS	1	mos and interlayer and barrier and seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 00:48			0
4	BRS	11	gate and interlayer and barrier with seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 00:49			0
5	BRS	68	gate and interlayer and barrier and seed and capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/09/08 21:43			0